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EXAMINER	
KAO, WEI PO ERIC	

ART UNIT	PAPER NUMBER
2416	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/797,379	TAYLOR ET AL.	
	Examiner	Art Unit	
	WEI-PO KAO	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-15,18 and 19* is/are rejected.

7)☒ Claim(s) *3,4,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Pre-Brief Appeal Conference decision

1. The prosecution is reopened.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 8, 12 and 15 have been considered but are moot in view of the new ground(s) of rejection.

In view of the Amendment/Remarks filed on 02/04/2008, applicants' arguments have been considered but are moot in view of the new ground(s) or rejection. The action is made final based on the presented amendment, which necessitated the new ground(s) of rejection.

Note: previous rejections, mailed on 05/13/2008, have been withdrawn.

Claim Rejection - 35 USC § 103

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 5, 6, 7, 8, 9, 10, 12, 13, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Demetrescu et al, U.S. Patent No. 7146312 (Demetrescu) in view of Krishnarajah et al, U.S. Publication No. 2003/0081592 (Krishnarajah).

Regarding Claim 1, Demetrescu teaches that **a method in a packet switched data transfer system for processing header bits and payload bits in a frame of bits, the method comprising** (see Abstract, Figure 12, 13, 18 and 19, Column 2 Lines 4-15, Column 3 Lines 50-67, Column 4 Lines 23-25, Column 12 Lines 24 63-67, Column 13 Lines 1-14, Column 18 Lines 20 54-67, Column 19 Lines 1-3 e.g. an encoding method for processing header bits and payload bits in a block, which is essentially a frame comprising headers and payloads of multiple sub frames)**, implying that classifying each of the header bits in the frame into a first predetermined class of bits and into a second predetermined class of bits; implying that classifying each of the payload bits in the frame into the first predetermined class of bits and into the second predetermined class of bits** (see Figures 13(a) and 19(a), Column 19 Lines

4-7 i.e. according to figure 19(a), fields of the block (a frame essentially), which contains headers and payloads of two different frames belonging to two different users, are arranged according to the two different frames/users, which are as two different predetermined classes: frame 1/user 1 V.S. frame 2/user 2; specifically the fields representing the header of the frame are arranged/classified into the first predetermined class and into the second predetermined class; since each field, such as USF 1 and HDR 1 for frames 1/user 1 for example, contains certain number of bits, each of the header bits in the frame is classified into the first predetermined class of bits and into the second predetermined class of bits; similarly, each of the payload bits in the frame is classified into the first predetermined class of bits and into the second predetermined of bits)**; processing the first predetermined class of bits, in the frame, in accordance with a first predetermined mechanism; and processing the second predetermined class of bits in accordance with a second predetermined mechanism** (see Figures 13(a) and 19(a), Column 19 Lines 4-7 i.e. according to column 19 lines 4-7, frame 13(a) is rearranged as frame 19(a); similarly, the process of rearranging the fields of the frame can be reversed, namely 19(a) can also be rearranged as 13(a); when rearranging 19(a) to form 13(a), all fields are rearranged according to the first predetermined class and the second predetermined class, namely the header and payload of the frame 1 are grouped together and the header and payload of the frame 2 are grouped together; since each field, such as HDR 1, CLASS I (1) and CLASS II (1), contains certain number of bits, the first predetermined class of bits, in the frame, are processed in accordance with a first predetermined mechanism; the second predetermined class of bits, in the frame, are processed in accordance with a first predetermined mechanism). While Demetrescu implies the teaching of classifying header and payload bits into two classes, Demetrescu does not

explicitly teaches that **classifying each of the header bits in the frame into a first predetermined class of bits and into a second predetermined class of bits; classifying each of the payload bits in the frame into the first predetermined class of bits and into the second predetermined class of bits.** Krishnarajah from the same field of endeavor teach that **classifying each of the header bits in the frame into a first predetermined class of bits and into a second predetermined class of bits; classifying each of the payload bits in the frame into the first predetermined class of bits and into the second predetermined class of bits** (see Abstract, Figure 3, [0007-0008] [0036] e.g. [0036] lines 1-9; accordingly Krishnarajah teaches that bits of a frame, which includes at least a header and a payload, are classified into two classes)**.** Krishnarajah also teaches that **processing the first predetermined class of bits, in the frame, in accordance with a first predetermined mechanism; and processing the second predetermined class of bits in accordance with a second predetermined mechanism** (see Figure 3, [0007-0008] [0036] e.g. [0036] lines 1-9; grouping the bits of the same class; Krishnarajah's grouping mechanism also suggests that revering the arrangement from frame 19(a) to 13(a) in Demetrescu's invention is possible). At the time of the invention, it would have been obvious to a person ordinary skill in the art to also adopt Krishnarajah's bit-classifying mechanism and implement Krishnarajah's classified-frame processing mechanism with Demetrescu's frame processing system. The motivation would have been that it is desired to provide high quality of service in processing frame, which may contain different types of data or information (see Krishnarajah [0006]).

Regarding Claim 2, Demetrescu further teaches that **the method, further comprising: constructing a new frame of bits based upon the processed first predetermined class of bits and the processed second predetermined class of bits** (see Column 19 Lines 4-7 i.e. when frame 19(a) is rearranged to form frame 13(a)).

Regarding Claim 5, Krishnarajah further teaches that **the method, wherein: processing the first predetermined class of bits in accordance with the first predetermined mechanism includes grouping the first predetermined class of bits; and processing the second predetermined class of bits in accordance with the second predetermined mechanism includes grouping the second predetermined class of bits** (see [0036]). At the time of the invention, it would have been obvious to a person ordinary skill in the art to also adopt Krishnarajah's bit-classifying mechanism and implement Krishnarajah's classified-frame processing mechanism with Demetrescu's frame processing system. The motivation would have been that it is desired to provide high quality of service in processing frame, which may contain different types of data or information (see Krishnarajah [0006]).

Regarding Claim 6, Demetrescu teaches that **the method, further comprising: constructing a new frame of bits based upon the grouped-processed first predetermined class of bits and the grouped-processed second predetermined class of bits** (see Column 19 Lines 4-7 i.e. when frame 19(a) is rearranged to form frame 13(a)). However, Demetrescu does not teach that **the method, further comprising: grouping the processed first predetermined class of bits;**

grouping the processed second predetermined class of bits. Krishnarajah from the same field of endeavor teaches that **the method, further comprising: grouping the processed first predetermined class of bits; grouping the processed second predetermined class of bits** (see [0036]). At the time of the invention, it would have been obvious to a person ordinary skill in the art to also adopt Krishnarajah's bit-classifying mechanism and implement Krishnarajah's classified-frame processing mechanism with Demetrescu's frame processing system. The motivation would have been that it is desired to provide high quality of service in processing frame, which may contain different types of data or information (see Krishnarajah [0006]).

Regarding Claim 7, Krishnarajah further teaches that **the method, wherein: the first predetermined mechanism includes applying a first error protection algorithm, and the second predetermined mechanism includes applying a second error protection algorithm** (see [0009]). At the time of the invention, it would have been obvious to a person ordinary skill in the art to apply different error protection algorithms to different class of frame bits. The rationale would have been that it is desired to provide different protection to different type of class of bits in order to fulfill different QoS.

Regarding Claim 8, Demetrescu teaches that **a method in a packet switched data transfer system for reducing an encoded frame size a frame having header bits and payload bits, the method comprising** (see Abstract, Figure 12, 13, 18 and 19, Column 2 Lines 4-15, Column 3 Lines 50-67, Column 4 Lines 23-25, Column 12 Lines 24 63-67, Column 13 Lines 1-14, Column

18 Lines 20 54-67, Column 19 Lines 1-3 e.g. an encoding method for processing header bits and payload bits in a block, which is essentially a frame comprising headers and payloads of multiple sub frames)**, implying that classifying each of the header bits in the frame into a first predetermined class of bits and into a second predetermined class of bits; implying that classifying each of the payload bits in the frame into the first predetermined class of bits and into the second predetermined class of bits** (see Figures 13(a) and 19(a), Column 19 Lines 4-7 i.e. according to figure 19(a), fields of the block (a frame essentially), which contains headers and payloads of two different frames belonging to two different users, are arranged according to the two different frames/users, which are as two different predetermined classes: frame 1/user 1 V.S. frame 2/user 2; specifically the fields representing the header of the frame are arranged/classified into the first predetermined class and into the second predetermined class; since each field, such as USF 1 and HDR 1 for frames 1/user 1 for example, contains certain number of bits, each of the header bits in the frame is classified into the first predetermined class of bits and into the second predetermined class of bits; similarly, each of the payload bits in the frame is classified into the first predetermined class of bits and into the second predetermined of bits)**; encoding the first predetermined class of bits, in the frame, in accordance with a first predetermined mechanism; and encoding the second predetermined class of bits, in the frame, in accordance with a second predetermined mechanism; wherein the first encoding process is same from the second encoding process** (see Figure 19(b), Column 19 Lines 7-34 i.e. according to column 19 lines 7-43, encoding process for 19(a) is the same regardless the sections being as classified frame 1 or frame 2)**.** While Demetrescu implies the teaching of classifying header and payload bits into two classes, Demetrescu does not explicitly teaches that

classifying each of the header bits in the frame into a first predetermined class of bits and into a second predetermined class of bits; classifying each of the payload bits in the frame into the first predetermined class of bits and into the second predetermined class of bits. Demetrescu also does not teach that **wherein the first encoding process is different from the second encoding process.** Krishnarajah from the same field of endeavor teach that **classifying each of the header bits in the frame into a first predetermined class of bits and into a second predetermined class of bits; classifying each of the payload bits in the frame into the first predetermined class of bits and into the second predetermined class of bits** (see Abstract, Figure 3, [0007-0008] [0036] e.g. [0036] lines 1-9; accordingly Krishnarajah teaches that bits of a frame, which includes at least a header and a payload, are classified into two classes); **wherein the first encoding process is different from the second encoding process** (see Figure 3, [0007-0008] [0036] e.g. [0036] lines 9-19; each group of classified bits is encoded with a corresponding header, which identifies the group's treatment class; in another word, each group of classified bits is encoded with additional information to identify the group's treatment class and such additional information is different for each group of bits). At the time of the invention, it would have been obvious to a person ordinary skill in the art to also adopt Krishnarajah's bit-classifying mechanism and implement Krishnarajah's classified-frame processing mechanism with Demetrescu's frame processing system. The motivation would have been that it is desired to provide high quality of service in processing frame, which may contain different types of data or information (see Krishnarajah [0006]).

Regarding Claim 9, Demetrescu further teaches that **the method, further comprising: constructing a new frame based upon the encoded first predetermined class of bits and the encoded second predetermined class of bits** (see Column 19 Lines 4-7 i.e. when frame 19(a) is rearranged to form frame 13(a)).

Regarding Claim 10, Demetrescu teaches that **the method, further comprising: constructing a new frame of bits based upon the grouped encoded first predetermined class of bits and the grouped encoded second predetermined class of bits** (see Column 19 Lines 4-7 i.e. when frame 19(a) is rearranged to form frame 13(a)). However, Demetrescu does not teach that **the method, further comprising: grouping the encoded first predetermined class of bits; grouping the encoded second predetermined class of bits.** Krishnarajah from the same field of endeavor teaches that **the method, further comprising: grouping the processed first encoded class of bits; grouping the encoded second predetermined class of bits** (see [0036]). At the time of the invention, it would have been obvious to a person ordinary skill in the art to also adopt Krishnarajah's bit-classifying mechanism and implement Krishnarajah's classified-frame processing mechanism with Demetrescu's frame processing system. The motivation would have been that it is desired to provide high quality of service in processing frame, which may contain different types of data or information (see Krishnarajah [0006]).

Regarding Claim 12, Demetrescu teaches that **a method in a packet switched data transfer system for reformatting a frame having header bits and payload bits, the method**

comprising (see Abstract, Figure 12, 13, 18 and 19, Column 2 Lines 4-15, Column 3 Lines 50-67, Column 4 Lines 23-25, Column 12 Lines 24 63-67, Column 13 Lines 1-14, Column 18 Lines 20 54-67, Column 19 Lines 1-3 e.g. an encoding method for processing header bits and payload bits in a block, which is essentially a frame comprising headers and payloads of multiple sub frames)**, implying that classifying each of the header bits in the frame into a first predetermined class of bits and into a second predetermined class of bits; implying that classifying each of the payload bits in the frame into the first predetermined class of bits and into the second predetermined class of bits** (see Figures 13(a) and 19(a), Column 19 Lines 4-7 i.e. according to figure 19(a), fields of the block (a frame essentially), which contains headers and payloads of two different frames belonging to two different users, are arranged according to the two different frames/users, which are as two different predetermined classes: frame 1/user 1 V.S. frame 2/user 2; specifically the fields representing the header of the frame are arranged/classified into the first predetermined class and into the second predetermined class; since each field, such as USF 1 and HDR 1 for frames 1/user 1 for example, contains certain number of bits, each of the header bits in the frame is classified into the first predetermined class of bits and into the second predetermined class of bits; similarly, each of the payload bits in the frame is classified into the first predetermined class of bits and into the second predetermined of bits)**; grouping the classified header bits of the first predetermined class of bits with the classified payload bits of the first predetermined class of bits; grouping the classified header bits of the second predetermined class of bits with the classified payload bits of the second predetermined class of bits** (see Figures 13(a) and 19(a), Column 19 Lines 4-7 i.e. according to column 19 lines 4-7, frame 13(a) is rearranged as frame 19(a); similarly, the process

of rearranging the fields of the frame can be reversed, namely 19(a) can also be rearranged as 13(a); when rearranging 19(a) to form 13(a), all fields are rearranged according to the first predetermined class and the second predetermined class, namely the header and payload of the frame 1 are grouped together and the header and payload of the frame 2 are grouped together; since each field, such as HDR 1, CLASS I (1) and CLASS II (1), contains certain number of bits, the first predetermined class of bits, in the frame, are processed in accordance with a first predetermined mechanism; the second predetermined class of bits, in the frame, are processed in accordance with a first predetermined mechanism); **constructing a reformatted frame using the grouped first predetermined class of bits and the grouped second predetermined class of bits** (see Figure 13(a) i.e. frame 19(a) can be rearranged to form frame 13(a)). While Demetrescu implies the teaching of classifying header and payload bits into two classes, Demetrescu does not explicitly teaches that **classifying each of the header bits in the frame into a first predetermined class of bits and into a second predetermined class of bits; classifying each of the payload bits in the frame into the first predetermined class of bits and into the second predetermined class of bits.** Krishnarajah from the same field of endeavor teaches that **classifying each of the header bits in the frame into a first predetermined class of bits and into a second predetermined class of bits; classifying each of the payload bits in the frame into the first predetermined class of bits and into the second predetermined class of bits** (see Abstract, Figure 3, [0007-0008] [0036] e.g. [0036] lines 1-9; accordingly Krishnarajah teaches that bits of a frame, which includes at least a header and a payload, are classified into two classes). Krishnarajah also teaches that **grouping the classified header bits of the first predetermined class of bits with the classified payload bits of the first**

predetermined class of bits; grouping the classified header bits of the second predetermined class of bits with the classified payload bits of the second predetermined class of bits (see Figure 3, [0007-0008] [0036] e.g. [0036] lines 1-9; grouping the bits of the same class; Krishnarajah's grouping mechanism also suggests that revering the arrangement from frame 19(a) to 13(a) in Demetrescu's invention is possible). At the time of the invention, it would have been obvious to a person ordinary skill in the art to also adopt Krishnarajah's bit-classifying mechanism and implement Krishnarajah's classified-frame processing mechanism with Demetrescu's frame processing system. The motivation would have been that it is desired to provide high quality of service in processing frame, which may contain different types of data or information (see Krishnarajah [0006]).

Regarding Claim 13, Demetrescu teaches that **the method of claim 12, further comprising: constructing a reformatted frame includes constructing a reformatted frame using the encoded grouped first predetermined class of bits and the encoded grouped second predetermined class of bits** (see Column 19 Lines 4-7 i.e. when frame 19(a) is rearranged to form frame 13(a)). However, Demetrescu does not teach that **the method, further comprising: before constructing a reformatted frame, encoding the grouped first predetermined class of bits with a first predetermined algorithm; and encoding the grouped second predetermined class of bits with a second predetermined algorithm.** Krishnarajah from the same field of endeavor teaches that **the method, further comprising: before constructing a reformatted frame, encoding the grouped first predetermined class of bits with a first predetermined algorithm; and encoding the grouped second predetermined class of bits with a second**

predetermined algorithm (see [0036]). At the time of the invention, it would have been obvious to a person ordinary skill in the art to also adopt Krishnarajah's bit-classifying mechanism and implement Krishnarajah's classified-frame processing mechanism with Demetrescu's frame processing system. The motivation would have been that it is desired to provide high quality of service in processing frame, which may contain different types of data or information (see Krishnarajah [0006]).

Regarding Claim 15, Demetrescu teaches that **a packet switched data transfer device comprising** (see Abstract, Figure 12, 13, 18 and 19, Column 2 Lines 4-15, Column 3 Lines 50-67, Column 4 Lines 23-25, Column 12 Lines 24 63-67, Column 13 Lines 1-14, Column 18 Lines 20 54-67, Column 19 Lines 1-3 e.g. figures 12 and 18; a RLC/MAC block generating circuitry for processing header bits and payload bits in a block, which is essentially a frame comprising headers and payloads of multiple sub frames); **a frame receiver configured to receive a frame of bits, the frame of bits comprising a plurality of header bits and a plurality of payload bits** (see Figures 12, 13, 18 and 19, Column 12 Lines 25-62, Column 18 Lines 21-53 e.g. figures 12 and 13)**; a bit processor configured to process the bits, in the frame, according to a first predetermined process and to process the bits, in the frame, according to a second predetermined process** (see Figures 12 and 13, Column 12 Lines 25-62, Column 18 Lines 21-53). However, Demetrescu does not teach that **a bit classifier coupled to the frame receiver, the bit classifier configured to classify each of the plurality of header bits and each of the plurality of payload bits into a first class of bits and into a second class of bits** see Figure 3, [0007-0008] [0036] e.g. figure 3 elements 30 and 32; [0036] lines 1-9)**; a bit processor coupled**

to the bit classifier, the bit processor configured to process the classified first class of bits, in the frame, according to a first predetermined process and to process the classified second class of bits, in the frame, according to a second predetermined process (see Figure 3, [0036] Lines 9-19 e.g. figure 3 element 36)**.** At the time of the invention, it would have been obvious to a person ordinary skill in the art to also adopt Krishnarajah's bit-classifying mechanism and implement Krishnarajah's classified-frame processing mechanism with Demetrescu's frame processing system. The motivation would have been that it is desired to provide high quality of service in processing frame, which may contain different types of data or information (see Krishnarajah [0006]).

Regarding Claim 19, Demetrescu further teaches that **the packet switched data transfer device, further comprising: a frame constructor coupled to the bit processor, the frame constructor configured to construct a new frame of bits based upon the processed first class of bits and the processed second class of bits** (see Column 19 Lines 4-7 i.e. when frame 19(a) is rearranged to form frame 13(a))**.**

7. Claims 11, 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Demetrescu et al, U.S. Patent No. 7146312 (Demetrescu) in view of Krishnarajah et al, U.S. Publication No. 2003/0081592 (Krishnarajah) as applied to claim 8, 13 and 15 above, and further in view of Gersho et al, U.S. Patent No. 6625226 (Gersho).

Regarding Claim 11, Demetrescu and Krishnarajah teach all the limitations in claim 8 except that **the method, wherein the first predetermined encoding process has a first coding rate greater than a second coding rate of the second predetermined encoding process.** Gersho from the same field of endeavor teach that **the method, wherein the first predetermined encoding process has a first coding rate greater than a second coding rate of the second predetermined encoding process** (see Abstract, Column 4 e.g. column 4 lines 34-35)**.** At the time of the invention, it would have been obvious to a person ordinary skill in the art to encode different data at different rate. The motivation would have been that better tradeoff between coding rate and throughput rate is obtainable (see column 4 lines 1-5).

Regarding Claim 11, Demetrescu and Krishnarajah teach all the limitations in claim 13 except that **the method, wherein the first predetermined algorithm has a first coding rate greater than a second coding rate of the second predetermined algorithm.** Gersho from the same field of endeavor teach that **the method, wherein the first predetermined algorithm has a first coding rate greater than a second coding rate of the second predetermined algorithm** (see Abstract, Column 4 e.g. column 4 lines 34-35)**.** At the time of the invention, it would have been obvious to a person ordinary skill in the art to encode different data at different rate. The motivation would have been that better tradeoff between coding rate and throughput rate is obtainable (see column 4 lines 1-5).

Regarding Claim 18, Demetrescu and Krishnarajah teach all the limitations in claim 8 except that **the packet switched data transfer device, wherein: the first predetermined process has a first coding rate, and the second predetermined process has a second coding rate, the second coding rate less than the first coding rate.** Gersho from the same field of endeavor teach that **the packet switched data transfer device, wherein: the first predetermined process has a first coding rate, and the second predetermined process has a second coding rate, the second coding rate less than the first coding rate** (see Abstract, Column 4 e.g. column 4 lines 34-35)**.** At the time of the invention, it would have been obvious to a person ordinary skill in the art to encode different data at different rate. The motivation would have been that better tradeoff between coding rate and throughput rate is obtainable (see column 4 lines 1-5).

Allowable Subject Matter

8. Claims 3, 4, 16 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

For claim 3, 4, 16 and 17, prior art fails to show alone or in combination the outing queue step of classifying header bits based upon a location of the header bits in the frame; payload bits based upon a location of the payload bits in the frame; header bits based upon a pre-assigned header weight of the header bits; payload bits based upon a pre-assigned header weight of the payload bits.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Referring to the PTO Form 892, references are cited to show similar method and system of classifying bits of information.

12. Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WEI-PO KAO whose telephone number is (571)270-3128. The examiner can normally be reached on Monday through Friday, 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571)272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ricky Ngo/

Supervisory Patent Examiner, Art Unit 2416

/Wei-po Kao/

Examiner, Art Unit 2416